**Implementation of CRC on FPGA**

Abstract

All real systems that work with digitally represented data require error detecting codes because all real channels are noisy to some extent. The basic goal is to detect errors in data transmission over unreliable or noisy communication channels. Encoding and decoding techniques play a major role in digital communication as the received bit stream usually contains a number of errors. Cyclic Redundancy Codes (CRCs) provide a first line of defence against data corruption in many networks. The basic goal is to control errors in data transmission over unreliable or noisy communication channels. CRC code provides a simple, yet powerful, method for the detection of burst errors during digital data transmission and storage. In this paper simulation is shown and implementation of CRC-32 is done on FPGA.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis